UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/751,714	01/05/2004	Wing K. Luk	YOR920030603US1	2257

48062 7590 05/11/2007

RYAN, MASON & LEWIS, LLP
1300 POST ROAD
SUITE 205
FAIRFIELD, CT 06824

EXAMINER	
MONDT, JOHANNES P	

ART UNIT	PAPER NUMBER
3663	

MAIL DATE	DELIVERY MODE
05/11/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/751,714	LUK ET AL.	
	Examiner	Art Unit	
	Johannes P. Mondt	3663	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 February 2007 and 06 November 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-37* is/are pending in the application.

4a) Of the above claim(s) *21-23 and 29-35* is/are withdrawn from consideration.

5)☒ Claim(s) *3-8,17-20,36 and 37* is/are allowed.

6)☒ Claim(s) *1,2 and 9-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 December 2005* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Applicant's election with traverse of the Group I invention in the reply filed on 2/21/07 is acknowledged. The traversal is on the ground(s) that no serious burden would exist. This is not found persuasive because examiner explained that a serious burden exists for very specific reasons, i.e., because of the different classification, - actually different classes, for Group I and Group II, and because of the alternative use of the product. Applicant did not respond to said very specific reasons.

Therefore, the requirement is still deemed proper and is therefore made FINAL.

Accordingly, claims 21-23 and 29-35 have been withdrawn from consideration.

Response to Amendment

Amendment filed 11/06/06 in conjunction with said Reply filed 2/21/07 forms the basis for this action. Comments on Remarks submitted with said Amendment are included below under "Response to Arguments".

Drawings

Figure 1A, 1B, 1C, 4A, 4B, 6 and 8 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page

header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

1. ***Claim 12*** is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim contains subject matter not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. In particular, a gate diode otherwise defined by claim 12 with the source diffusion region abutting the gate and drain diffusion region abutting another side of gate wherein the second terminal is coupled to the source diffusion region and wherein the first terminal is coupled to the gate is not AND CANNOT BE a two-terminal semiconductor device but instead a one-terminal semiconductor device, because source/drain and gate are short-circuited.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. ***Claims 1-2, 9-10 and 13-15*** are rejected under 35 U.S.C. 102(b) as being anticipated by Mead et al (5,844,265). With reference to the rejection above under 35 USC 112, second paragraph, examination is carried out assuming "adapted to amplify said signal" means "placed in an environment wherein said signal is amplified" while no amplifying function other than an inherent one as capacitor (through attraction of charges by a control signal on one of its two terminals leading to a larger voltage change on the other terminal) is assumed involved in any adaptation.

Mead et al teach (title, abstract, Figures 1, 3, 6, 7, and 9; cols. 2-10) a circuit 10 (col. 2, l. 65) for amplifying signals (abstract, first sentence), the circuit comprising:

a control line (LOAD BIAS connected to a bias voltage source) (cf. col. 3, l. 10-20 and Fig. 7); and

a two terminal semiconductor device 62-1 (MOS transistor used as varactor with source and drain short-circuited: col. 3, l. 33-43; cf. Fig. 1, 9 included as 62-1, 62-2, in Fig. 7), having first and second terminals (loc.cit.), the first terminal (gate of gated diode 62-2) coupled to a signal line 194-1 (of sense amplifier 10), and the second terminal coupled to the control line (capacitively, through 16-1) (loc.cit.), wherein the two terminal semiconductor device is adapted to have a capacitance (gate-channel/source/drain capacitance) when a voltage on the first terminal

relative to the second terminal is in a first voltage range and to have a lower capacitance when the voltage on the first terminal relative to the second terminal is in a second voltage range (because the MOS varactor = gated diode inherently has a variable capacitor, wherein the gate voltage can be raised or lowered (depending on the conductivity type of the varactor) to cause depletion, and even further to cause inversion of the channel),

wherein the control line is adapted to be coupled to a control signal (through the capacitive coupling to the aforementioned bias voltage source); and

wherein the signal line is adapted to be coupled to a signal (from the vertical scanner) and to be an output of the circuit (through 218) (col. 8, l. 44-col. 9, l. 64), and wherein the two-terminal semiconductor device is CAPABLE of amplifying said signal in response to a substantial change in voltage of said control signal: by admission by applicant, Figure 11A of disclosure: any amplifying function must be across the node of 1101/1110 and hence is inherent as a property of *capability* of said gate diode. In reference to the claim language referring to ""wherein the two-terminal semiconductor device is adapted to amplify", intended use and other types of functional language must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. In re

Casey,152 USPQ 235 (CCPA 1967); In re Otto , 136 USPQ 458, 459 (CCPA 1963).

Finally, the limitation "adapted" pertains itself to a method of making the device and as such constitutes a product-by-process limitation. The limitation "adapted" is only of patentable weight in as much as the method steps distinguish the final structure, and to the extent not impacting final structure are taken to be product-by-process limitations and non-limiting. A product by process claim is directed to the product per se, no matter how they are actually made. See In re Fessman, 180 USPQ 324, 326 (CCPA 1974); In re Marosi et al, 218 USPQ 289, 292 (Fed. Cir. 1983), and In re Thorpe, 227 USPQ 964, 966 (Fed. Cir. 1985), all of which make clear that it is the patentability of the final structure of the product "gleaned" from the process steps that must be determined in a "product-by-process" claim, and not the patentability of the process. See also MPEP 2113. Moreover, an old or obvious product produced by a new method is not a patentable product, whether claimed in "product by process" claims or not.

On claim 2: the two terminal semiconductor device by Mead et al comprises a gated diode 62-1 (also 32 in Fig. 1) (Fig. 7) having a well (N.B.: substrate is a p-well; col. 5, l. 1-5; Fig. 3) because it is implemented as p-type substrate 156 (Fig. 6 and col. 7, l. 65) in Fig. 6, which inherently is a (electrostatic potential) well for all majority charge carriers therein) and wherein the threshold voltage can inherently be modified by modifying a dopant level in said well of the gated diode because said dopant level determines the number of charge carriers (see, for instance, Wolf, ISBN 0-961672-5-3, pages 116-133).

On claim 9: the circuit further comprises an output circuit 206-1 / 216 (Fig.7) adapted to produce an output corresponding to a voltage at the gate input of the gated

diode (depending as it is on the capacitance of capacitor 62-1).

On claim 10: the output circuit comprises one or more of the following: a buffer, an inverter, and a latch, because the hold/sample circuit 206 (col. 9, l. 25-32) is a buffer circuit.

On claim 13: the two terminal semiconductor device comprises a gated diode 32 (62-1, 62-2) (col. 3, l. 33-43) (N.B.: source and drain both connected to the output of the sense amplifier and hence also to each other, forming one pole of the diode, the gate forming the other one).

On claims 14-15: the gated diode is an n-type gated diode (col. 3, l. 36) or a p-type gated diode (col. 3, l. 33-35), wherein the threshold voltage is a positive, respectively negative voltage (inherently, a positive voltage is required to cause inversion in the former, a negative voltage in the latter, wherein the two terminal semiconductor device is adapted to have a capacitance when a voltage on the first terminal relative to the second terminal is more positive, respectively negative, than the threshold voltage and to have a lower capacitance when the voltage on the first terminal is less positive, respectively negative, than the threshold voltage.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. ***Claim 11*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Mead et al as applied to claim 1, and in view of Ravi et al (US 2004/0263272 A1) and Brachitta et al (6,130,469).As detailed above, Mead et al anticipate claim 1. Mead et al do not teach the further limitation defined by claim 11 as a whole although they clearly teach a MOS n-channel transistor as the basis for their varactor 32, which inherently has an insulation formed between the gate and the well and a source region (see col. 3, l. 33-43), and although they clearly teach the first terminal is coupled to the gate and the second terminal is coupled to the source (see above, discussion of claim 1).

However, it would have been obvious to include said further limitation on overlapping of said source region "one side of the insulator and gate" in view of Ravi et al, who teach said overlap in a varactor to be non-zero so as to have a minimum capacitance in the OFF state (see [0066]). *Motivation* to include the teaching by Ravi et al derives from the resulting improved controllability of the ratios of capacitances in OFF and ON state in the varactor so as to have a more accurately quantified varactor.

Furthermore, it would have been obvious to include the limitation "a shallow trench isolation region abutting another side of the insulator and gate" in view of Brachitta et al, who teach said STI region to insulate MOS capacitors from

neighboring FET devices (col. 2, l. 13-23) thus making the devices independent as they should. *Motivation* to include the teaching by Brachitta et al in the invention by Mead et al derives from said advantage of device independence coupled with the presence in one wafer of several FETs and the varactor as MOS capacitor also in Mead et al (32 is varactor as MOS capacitor in wafer with FETs (col. 7, l. 3-36).

Response to Arguments

Applicant's arguments filed 11/06/06 have been fully considered but they are not persuasive.

First examiner regrets to have to withdraw allowability as indicated for claims 3-8, 24-28, 36 and 37 because of a double patenting rejection necessitated by US Patent 7,116,594 B2 to common inventors Luk and Dennard and to the same Assignee (IBM). This action is made Non-Final for this reason (only).

With regard to the traverse of the Objection to the Drawings, applicant himself admits in the Specification that said Drawings are conventional, because, counter to Applicant argument of traverse, "conventional" is an adjective to setting, not to Field Effect Transistor (such as would be the case in "conventional Field Effect Transistor's setting" or "setting of a conventional Field Effect Transistor"). Therefore, said Objection is maintained in the present action.

With regard to the proposed Amendment to the Specification, said proposed Amendment is approved.

With regard to the traverse of the rejection under 35 USC 112, first paragraph, of claim 12, said traverse fails to take into account that a short-circuit between source and gate and a short-circuit between drain and gate necessarily result from said source and drain diffusion regions abutting the gate as recited in claim 12. Therefore, the rejection of claim 12 under 35 USC 112, first paragraph because of the internal contradiction between the recited "two terminal" nature of the claimed "semiconductor device" and the short-circuiting of all terminal of an FET is maintained.

With regard to the rejection under 35 USC 112, second paragraph, of claims 1-2 and 9-16, the amendment to the claims has successfully overcome said rejection.

With regard to applicant's traverse of the rejection under 35 USC 102(b) over Mead et al (5,844,265) (pages 16-19):

Applicant's argument that Mead et al do not teach "a varactor utilized for performing amplification" (page 16), this is not a quote from the claim language, while Mead explicitly teaches his device to be for amplification (see office action and see Mead for element 10 identified as circuit for amplifying signals (col. 2, l. 61-65: it is a sense amplifier) while the stipulation "for amplifying signals" in the pre-amble constitutes functional language, and examiner refers in this regard to his comments on page 6, first paragraph, of the previous office action on the merits (mailed 8/4/06). While Applicant appears to admit that Mead et al teach a two-terminal device, applicant does not appear to believe that claim 1 recites a two-terminal device, although the claim language clearly and specifically recites

"a two terminal device" (line 6 of claim 1). Said traverse is thus not found persuasive.

With regard to applicant's traverse (central paragraph of page 16) that "each independent claim explicitly recites connecting such two-terminal devices in a certain way to perform signal amplification" does not find support in the claim language, claim 1 reciting only one two-terminal (semiconductor) device. Said traverse is thus found to be unpersuasive.

With regard to applicant's traverse that Mead does not teach an amplification control line (final paragraph of page 17 and the first and second paragraphs of page 18), the control line as identified by LOAD BIAS inherently is a control line, because it is a gate voltage. Said gate voltage is capable of giving off a control signal, namely a change in its voltage, which influences and hence controls the amplifier 10 because it influences the voltage at node 28, which applicant evidently agrees with. However, to exert control over the voltage in a portion of an amplifier 10 qualifies as control of said amplifier and hence said amplification when in use. Therefore, said traverse fails to persuade.

Finally, applicant's assertion that Mead is not capable of an amplification function since the LOAB BIAS is a DC signal is a matter of intended use at best (and hence even arguendo of zero patentable weight because a non-DC signal can easily be provided to it), while examiner cannot find any restriction to DC voltage in the patent by Mead et al. On the contrary, the LOAD BIAS 26 appears connected to a threshold voltage dependent voltage (col. 3, l. 10-20) and hence the LOAD BIAS must be capable of variation with said threshold voltage.

Because it is only the capability that has any patentable weight said traverse is not persuasive.

The remainder of applicant's arguments in traverse appears moot in view of the withdrawal of claim 21 from consideration and in view of the removal of the limitation "adapted".

Double Patenting

2. ***Claims 3 and 24*** are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 1 of U.S. Patent No. 7,116,594 B2. Although the conflicting claims are not identical, they are not patentably distinct from each other because of the following considerations:

Claim 1 of Patent 7,116,594 reads:

A sense amplifier circuit comprising:

an isolation device comprising a control terminal and first and second terminals, the first terminal of the isolation device coupled to a signal line;

a gated diode comprising first and second terminals, the first terminal of the gated diode coupled to the second terminal of the isolation device, and the second terminal of the gated diode coupled to a set line;

and

control circuitry coupled to the control terminal of the isolation device and adapted to control voltage on the control terminal of the isolation device in order to enable and disable the isolation device,

the control circuitry additionally coupled to the set line and adapted to control a voltage on the set line; wherein the signal line is adapted to be coupled to an input signal, and

wherein the second terminal of the isolation device is adapted to be used to derive an output for the sense amplifier circuit;

wherein said gated diode has a substantially large equivalent capacitance when a threshold voltage of said gated diode is a positive voltage and when a voltage on said first terminal relative to said second terminal is greater than said threshold voltage;

wherein said gated diode has a substantially small equivalent capacitance when said threshold voltage of said gated diode is a positive

voltage and when said voltage on said first terminal relative to said second terminal is not greater than said threshold voltage;

wherein said gated diode has a substantially large equivalent capacitance when said threshold voltage of said gated diode is a negative voltage and when a voltage on said first terminal relative to said second terminal is not greater than said threshold voltage; and wherein said gated diode has a substantially small equivalent capacitance when said threshold voltage of said gated diode is a negative voltage and when said voltage on said first terminal relative to said second terminal is greater than said threshold voltage.

Referring now to claim 3 of the current application,

with regard to the first paragraph, the claimed "circuit for amplifying signals" is met by the sense amplifier circuit of the patent; the claimed "control line" is inherent in the "control circuitry" of the patent; the claimed "two terminal semiconductor device having first and second terminals" is met by the "gated diode comprising first and second terminals" of the patent; the claimed "signal line" is met by the "second terminal of the isolation device", and the "second terminal coupled top the control line" is met by the "second terminal of the gate diode coupled to a set line" in the patent (N.B.: said set line has a voltage that evidently can be and is controlled: see "to control a voltage on the set line"); the limitations on first and second capacitance are inherent in a gate diode while control line and signal line are coupled to a control signal and output respectively according to lines 15-17 of claim 1 of the patent; and

with regard to the second paragraph of the claim language (claim 3 of the current application), the limitation "an isolation device intermediate the signal line and the two terminal semiconductor device" is met by claim 1 of the patent as it claims an isolation device with first terminal coupled to the signal line and

the second terminal coupled to a terminal of the gated diode (lines 2-3 and 3-4), "the isolation device having input, output and control terminal, the input of the isolation device coupled to the signal line and the output of the isolation device coupled to the first terminal, wherein the output of the isolation device is adapted to be the output of the circuit, and whereby the control terminal of the isolation device can be set to a control voltage" as claimed in the current application is met by the "control terminal of the isolation device", "the signal line is adapted to be coupled to an input signal" (line 15) and "the second terminal of the isolation device is adapted to be used to derive an output for the sense amplifier circuit" (lines 16-17) in the patent claim 1.

With regard to claim 24 of the current application, this method claim merely states the method of amplifying signals using the circuit of claim 3.

3. ***Claims 4-8, 17-20, 24-28 and 36-37*** are rejected on the ground of non-statutory double patenting over claims 1-35 of US Patent 7,116,594 B2 since the claims, if allowed, would improperly extend the "right to exclude" already granted in the patent.

The subject matter claimed in the instant application is fully disclosed in the patent and is covered by the patent because the patent and the application are claiming common subject matter: see isolation device as FET inherently having the capability to be turned on or off, and to isolate or conduct dependent upon the voltage on its terminals by virtue of having a threshold voltage (claims 4-6) and see Introduction on n-type and p-type FETs (claims 7-8); for claim 17 of the instant application see claim 3 of the patent; on claims 17-18 see control voltage

generator 890 (N.B.: a control voltage requires its generation whereas only the difference between control and reference voltage has physical significance); with regard to claims 18-20, for digital voltage produced by the reference voltage generator see first sentence of summary and ϕ (2221: Fig. 20) coupled to control voltage.2231 (loc.cit.); while with regard to claims 25-28 and 36-37 are obvious over the corresponding device claims 4-8 and otherwise also disclosed for the same reasons as given above.

Furthermore, there is no apparent reason why applicant was prevented from presenting claims corresponding to those of the instant application during prosecution of the application that matured into a patent. See In re Schneller, 397 F.2d 350, 158 USPQ 210 (CCPA 1968). See also MPEP § 804.

Allowable Subject Matter

4. ***Claim 16*** is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The following is a statement of reasons for the indication of allowable subject matter: within the context of claim 1 the differential circuit as recited in claim 16 has not been found in the prior art, nor has any prior art been found over which said differential circuit would have been obvious.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Johannes P. Mondt whose telephone number is 571-272-1919. The examiner can normally be reached on 8:00 - 18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack W. Keith can be reached on 571-272-6878. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JPM
May 9, 2007

Primary Patent Examiner:
/Johannes Mondt (Art Unit: 3663)